خازوق دوق ولم يقلع من ......الى ..........

// Write your modules here!

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module cp(cin,p,g,c0,c1);

input cin;

input[2:0]p,g;

output c0,c1;

assign c0=g[1]|(p[0]&cin&p[1])|(p[1]&g[0]);

assign c1=g[2]|(g[1]&p[2])|(p[0]&p[1]&g[0])|(cin &p[0]&p[1]&p[2]);

endmodule

//..........................

module FA0(a0,b0,cin,c1,sum0,p0,g0);

input cin ,a0 ,b0;

output c1,sum0,p0,g0;

assign p0=a0^b0;

assign g0=a0&b0;

assign sum0=a0^b0^cin;

assign c1=(a0&b0)|(a0&cin)|(b0&cin);

endmodule

//......................

module FA1(a0,b0,cin,sum0,p0,g0);

input cin ,a0 ,b0;

output sum0,p0,g0;

assign p0=a0^b0;

assign g0=a0&b0;

assign sum0=a0^b0^cin;

endmodule

//.............................

module FA3(a,b,cin,sum3,c);

input cin ,a ,b;

output sum3,c;

assign sum3=a^b^cin;

assign c=(a&b)|(a&cin)|(b&cin);

endmodule

//.............................

module circuit(a,b,s,cout,sel,flow);

input[3:0]a,b;

input sel;

output [3:0]s;

wire [2:0] c;

output cout,flow;

wire [3:0]w;

reg [2:0]p,g;

//to make b' when sel==1;

xor u(w[0],sel,b[0]);

xor u1(w[1],sel,b[1]);

xor u2(w[2],sel,b[2]);

xor u3(w[3],sel,b[3]);

FA0 v0(a[0],w[0],sel,c[0],s[0],p[0],g[0]);

FA1 v1(a[1],w[1],c[0],s[1],p[1],g[1]);

FA1 v5(a[2],w[2],c[1],s[2],p[2],g[2]);

cp carry\_ahead(sel,p,g,c[1],c[2]);

FA3 v6(a[3],w[3],c[2],s[3],cout);

xor(flow,cout,c[2]);

endmodule